TPS7A11 500-mA, Low V_{IN}, Low V_{OUT}, Ultra-Low Dropout Regulator

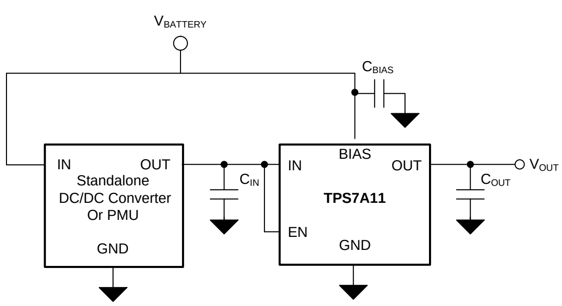
1 Features

- Ultra-Low Input Voltage Range: 0.75 V to 3.3 V
- Ultra-Low Dropout for Minimum Power Loss:
  - 140 mV (Maximum) at 500-mA DRV package
  - 110 mV (Maximum) at 500-mA YKA package
- Low Quiescent Current:
  - V_{IN} I_Q = 1.6 µA (Typical)
  - V_{BIAS} I_Q = 6 µA (Typical)
- 1.5% Accuracy Over Load, Line, and Temperature
- High PSRR: 64 dB at 1 kHz
- Available in Fixed-Output Voltages:
  - 0.5 V to 3.0 V (in 50-mV Steps)
- V_{BIAS} Range: 1.7 V to 5.5 V
- Packages:
  - 2.0-mm × 2.0-mm WSON (6)
  - 0.74-mm × 1.09-mm DSBGA (5)
- Active Output Discharge

2 Applications

- Smart Watch, Fitness Trackers
- Wireless Headphones and Earbuds
- Camera Modules
- Smart Phones and Tablets
- Portable Medical Devices
- Solid State Drives (SSDs)

Typical Application Circuit



3 Description

The TPS7A11 is an ultra-small, low quiescent current, low-dropout regulator (LDO). This device can source 500 mA with an outstanding ac performance (load and line transient responses). This device has an input range of 0.75 V to 3.3 V, and an output range of 0.5 V to 3.0 V with a very high accuracy of 1.5% over load, line, and temperature. This performance is ideal for supplying power to the lower core voltages of modern microcontrollers (MCUs) and analog sensors.

The primary power path is through the IN pin and can be connected to a power supply as low as 140 mV above the output voltage. This device supports very low input voltages with the use of an additional V_{BIAS} rail that is used to power the internal circuitry of the LDO. The IN and BIAS pins consume very low quiescent current of 1.6 µA and 6 µA, respectively. The low I_Q and ultra-low dropout features help to increase the efficiency of the solution in power-sensitive applications. For example, the supply voltage to the IN pin can be an output of a high-efficiency, DC/DC step-down regulator and the BIAS pin supply voltage can be a rechargeable battery.

The TPS7A11 is equipped with an active pulldown circuit to quickly discharge the output when disabled, and provides a known start-up state.

The TPS7A11 is available in a small 2.00-mm × 2.00-mm WSON, 6-pin (DRV) package and an ultra-small 0.74-mm × 1.09-mm, 5-pin DSBGA (YKA) package that makes the device suitable for space-constrained applications.

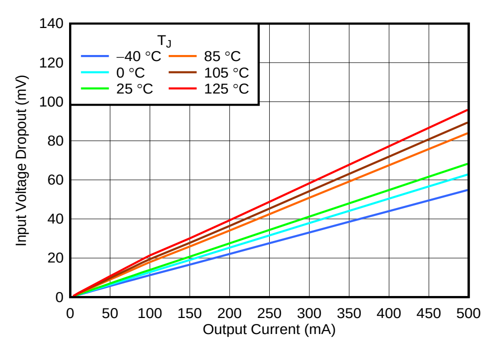
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS7A11	WSON (6)	2.00 mm × 2.00 mm
	DSBGA (5)(2)	0.74 mm × 1.09 mm (0.35-mm pitch)

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) Preview package.

Dropout vs I_{OUT} and Temperature, YKA Package



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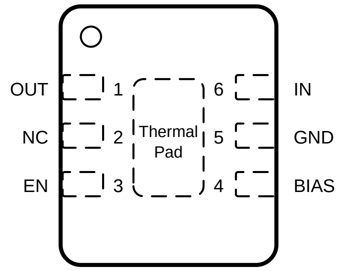
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2018	*	Initial release.

5 Pin Configuration and Functions

DRV Package
6-Pin SON With Exposed Thermal Pad
Top View



Not to scale

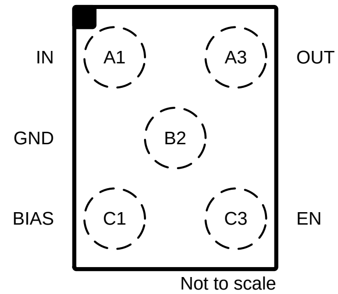
NOTE: TI recommends connecting the SON (DRV) package thermal pad to ground.

NOTE: NC – No internal connection.

Pin Functions: DRV

PIN		I/O	DESCRIPTION
NAME	NO.		
IN	6	Input	Input pin. A capacitor is required from IN to ground for stability. For best transient response, use the nominal recommended value or larger ceramic capacitor from IN to ground. Follow the recommended capacitor value as listed in the *Recommended Operating Conditions* table. Place the input capacitor as close to the input pin of the device as possible.
OUT	1	Output	Regulated output pin. A capacitor is required from OUT to ground for stability. For best transient response, use the nominal recommended value or larger ceramic capacitor from OUT to ground. Follow the recommended capacitor value as listed in the *Recommended Operating Conditions* table. Place the output capacitor as close to the output pin of the device as possible.
GND	5	—	Ground pin. This pin must be connected to ground.
BIAS	4	Input	BIAS pin. This pin enables the use of low-input voltage, low-output voltage (LILO) conditions. For best performance, use the nominal recommended value or larger ceramic capacitor from BIAS to ground. Follow the recommended capacitor value as listed in the *Recommended Operating Conditions* table. Place the bias capacitor as close to the bias pin of the device as possible.
EN	3	Input	Enable pin. Driving this pin to logic high enables the device. Driving this pin to logic low disables the device. If enable functionality is not required, this pin must be connected to IN or BIAS; however, connecting EN to IN is only acceptable if the IN pin voltage is greater than 0.9 V.
NC	2	—	This pin is not internally connected. Connect to ground for better thermal dissipation or leave floating.
Thermal pad		—	Connect the thermal pad to a large-area ground plane.

YKA Package (Preview)
5-Pin DSBGA
Top View



Pin Functions: YKA

PIN		I/O	DESCRIPTION
NO.[(1)]	NAME		
A1	IN	Input	Input pin. A capacitor is required from IN to ground for stability. For best transient response, use the nominal recommended value or larger ceramic capacitor from IN to ground. Follow the recommended capacitor value as listed in the *Recommended Operating Conditions* table. Place the input capacitor as close to the input pin of the device as possible.
A3	OUT	Output	Regulated output pin. A capacitor is required from OUT to ground for stability. For best transient response, use the nominal recommended value or larger ceramic capacitor from OUT to ground. Follow the recommended capacitor value as listed in the *Recommended Operating Conditions* table. Place the output capacitor as close to the output pin of the device as possible.
B2	GND	—	Ground pin. This pin must be connected to ground.
C1	BIAS	Input	BIAS pin. This pin enables the use of low-input voltage, low-output voltage (LILO) conditions. For best performance, use the nominal recommended value or larger ceramic capacitor from BIAS to ground. Follow the recommended capacitor value as listed in the *Recommended Operating Conditions* table. Place the bias capacitor as close to the bias pin of the device as possible.
C3	EN	Input	Enable pin. Driving this pin to logic high enables the device. Driving this pin to logic low disables the device. If enable functionality is not required, this pin must be connected to IN or BIAS; however, connecting EN to IN is only acceptable if the IN pin voltage is greater than 0.9 V.

(1) Preview package.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted.[(1)]

		MIN	MAX	UNIT
Voltage	Input, V_{IN}	–0.3	3.6	V
	Enable, V_{EN}	–0.3	6.0	
	Bias, V_{BIAS}	–0.3	6.0	
	Output, V_{OUT}	–0.3	V_{IN} + 0.3 [(2)]	
Current	Maximum output		Internally limited	A
Temperature	Operating junction, T_J	–40	150	°C
	Storage, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The absolute maximum rating is 3.6 V or (V_{IN} + 0.3 V), whichever is less.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	0.75		3.3	V
V_{BIAS}	Bias voltage	1.7		5.5	V
V_{OUT}	Output voltage	0.5		3.0	V
I_{OUT}	Peak output current	0		500	mA
C_{IN}	Input capacitor	2.2			µF
C_{BIAS}	Bias capacitor		0.1		µF
C_{OUT} (1)	Output capacitor	2.2		22	µF
T_J	Operating junction temperature	–40		125	°C

(1) Maximum ESR must be lower than 250 mΩ

6.4 Thermal Information

THERMAL METRIC (1)		TPS7A11		UNIT
		DRV (WSON)	YKA (DSBGA) (2)	
		6 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	77.3	169.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	91.6	1.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	41.1	55.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.3	1.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	41.0	55.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	18.6	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics application report* .
(2) Preview package

6.5 Electrical Characteristics

over T_J = –40°C to +125°C, $V_{IN} = V_{OUT(NOM)}$ + 0.5 V, $V_{BIAS} = V_{OUT(NOM)}$ + 1.4 V, I_{OUT} = 1 mA, V_{EN} = 1.0 V, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, and C_{BIAS} = 0.1 µF (unless otherwise noted); all typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Nominal accuracy	T_J = 25°C	-0.5		0.5	%
	Accuracy over temperature	–20°C ≤ T_J ≤ 85, DRV package $V_{OUT(NOM)}$ + 0.5 V ≤ V_{IN} ≤ 3.3 V, $V_{OUT(NOM)}$ + 1.4 V ≤ V_{BIAS} ≤ 5.5 V, 1 mA ≤ I_{OUT} ≤ 500 mA	-1.25		1.25	%
		–40°C ≤ T_J ≤ 85, YKA package $V_{OUT(NOM)}$ + 0.5 V ≤ V_{IN} ≤ 3.3 V, $V_{OUT(NOM)}$ + 1.4 V ≤ V_{BIAS} ≤ 5.5 V, 1 mA ≤ I_{OUT} ≤ 500 mA	-1.25		1.25	
		–40°C ≤ T_J ≤ 125, $V_{OUT(NOM)}$ + 0.5 V ≤ V_{IN} ≤ 3.3 V, $V_{OUT(NOM)}$ + 1.4 V ≤ V_{BIAS} ≤ 5.5 V, 1 mA ≤ I_{OUT} ≤ 500 mA	-1.5		1.5	
$\Delta V_{OUT} / \Delta V_{IN}$	V_{IN} line regulation	$V_{OUT(NOM)}$ + 0.5 V ≤ V_{IN} ≤ 3.3 V		0.001		%/V

Electrical Characteristics (continued)

over T_J = –40°C to +125°C, $V_{IN} = V_{OUT(NOM)}$ + 0.5 V, $V_{BIAS} = V_{OUT(NOM)}$ + 1.4 V, I_{OUT} = 1 mA, V_{EN} = 1.0 V, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, and C_{BIAS} = 0.1 µF (unless otherwise noted); all typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\Delta V_{OUT} / \Delta V_{BIAS}$	V_{BIAS} line regulation	$V_{OUT(NOM)}$ + 1.4 V ≤ V_{BIAS} ≤ 5.5 V		0.03		%/V
$\Delta V_{OUT} / \Delta I_{OUT}$	Load regulation	0.1 mA ≤ I_{OUT} ≤ 500 mA		0.2		%/A
$I_{Q(BIAS)}$	Bias pin current	T_J = 25°C, I_{OUT} = 0 mA	3	6	8	µA
		–40°C < T_J < 85°C, I_{OUT} = 0 mA			11	
		I_{OUT} = 0 mA			14	
		I_{OUT} = 500 mA			60	
$I_{Q(IN)}$	Input pin current (1)	T_J = 25°C, I_{OUT} = 0 mA		1.6	2.1	µA
		–40°C < T_J < 85°C, I_{OUT} = 0 mA			2.3	
		I_{OUT} = 0 mA			2.6	
		I_{OUT} = 500 mA			11	
$I_{SHDN(BIAS)}$	V_{BIAS} shutdown current	–40°C < T_J < 85°C, V_{IN} = 3.3 V, V_{BIAS} = 5.5 V, V_{EN} ≤ 0.4 V			400	nA
		–40°C < T_J < 125°C, V_{IN} = 3.3 V, V_{BIAS} = 5.5 V, V_{EN} ≤ 0.4 V			1200	
$I_{SHDN(IN)}$	V_{IN} shutdown current	–40°C < T_J < 85°C, V_{IN} = 3.3 V, V_{BIAS} = 5.5 V, V_{EN} ≤ 0.4 V			1	µA
		–40°C < T_J < 125°C, V_{IN} = 3.3 V, V_{BIAS} = 5.5 V, V_{EN} ≤ 0.4 V			3	
I_{CL}	Output current limit	V_{OUT} = 0.9 × $V_{OUT(NOM)}$, YKA Package	625	900	1150	mA
		V_{OUT} = 0.9 × $V_{OUT(NOM)}$, DRV Package	700	990	1250	
I_{SC}	Short circuit current limit	V_{OUT} = 0 V		300		mA
$V_{DO(IN)}$	V_{IN} dropout voltage (2)	$V_{IN} = V_{OUT(NOM)}$ – 0.1 V, I_{OUT} = 500 mA, YKA package		70	110	mV
		$V_{IN} = V_{OUT(NOM)}$ – 0.1 V, I_{OUT} = 500 mA, DRV package		90	140	
$V_{DO(BIAS)}$	V_{BIAS} dropout voltage (2)	I_{OUT} = 500 mA		0.85	1.2	V
		I_{OUT} = 250 mA		0.75	1.0	
V_{IN} PSRR	V_{IN} power-supply rejection ratio	f = 1 kHz, V_{OUT} = 1.0 V, I_{OUT} = 50 mA		64		dB
		f = 100 kHz, V_{OUT} = 1.0 V, I_{OUT} = 50 mA		37		
		f = 1 MHz, V_{OUT} = 1.0 V, I_{OUT} = 50 mA		31		
		f = 1.5 MHz, V_{OUT} = 1.0 V, I_{OUT} = 50 mA		35		
V_{BIAS} PSRR	V_{BIAS} power-supply rejection ratio	f = 1 kHz, V_{OUT} = 1.0 V, I_{OUT} = 500 mA		56		dB
		f = 100 kHz, V_{OUT} = 1.0 V, I_{OUT} = 500 mA		43		
		f = 1 MHz, V_{OUT} = 1.0 V, I_{OUT} = 500 mA		33		
V_n	Output voltage noise	Bandwidth = 10 Hz to 100 kHz, V_{OUT} = 1.0 V, I_{OUT} = 50 mA		93.9		μV_{RMS}
$V_{UVLO(BIAS)}$	Bias supply UVLO	V_{BIAS} rising	1.46	1.54	1.63	V
		V_{BIAS} falling	1.35	1.44	1.55	
$V_{UVLO\_HYST(BIAS)}$	Bias supply hysteresis	V_{BIAS} hysteresis		80		mV

(1) This current flowing from V_{IN} to GND.
(2) Dropout is not measured for V_{OUT} < 1.0 V.

Electrical Characteristics (continued)

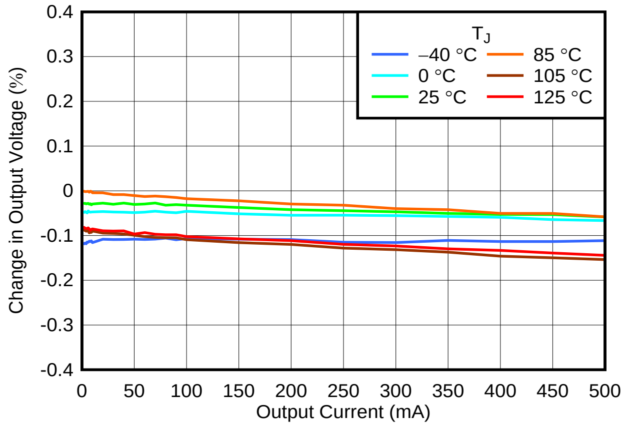
over T_J = –40°C to +125°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V, V_{BIAS} = $V_{OUT(NOM)}$ + 1.4 V, I_{OUT} = 1 mA, V_{EN} = 1.0 V, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, and C_{BIAS} = 0.1 µF (unless otherwise noted); all typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{UVLO(IN)}$	Input supply UVLO	V_{IN} rising	645	675	710	mV
		V_{IN} falling	565	600	640	
$V_{UVLO\_HYST(IN)}$	Input supply hysteresis	V_{IN} hysteresis		75		mV
t_{STR}	Start-up time(3)			525	1200	µs
$V_{HI(EN)}$	EN pin logic high voltage		0.9			V
$V_{LO(EN)}$	EN pin logic low voltage				0.4	V
I_{EN}	EN pin current	EN = 5.5 V		10		nA
$R_{PULLDOWN}$	Pulldown resistor	V_{BIAS} = 3.3 V, P version only		120		Ω
T_{SD}	Thermal shutdown temperature	Shutdown, temperature rising		160		°C
		Reset, temperature falling		145		

(3) Startup time = time from EN assertion to 0.95 × $V_{OUT(NOM)}$.

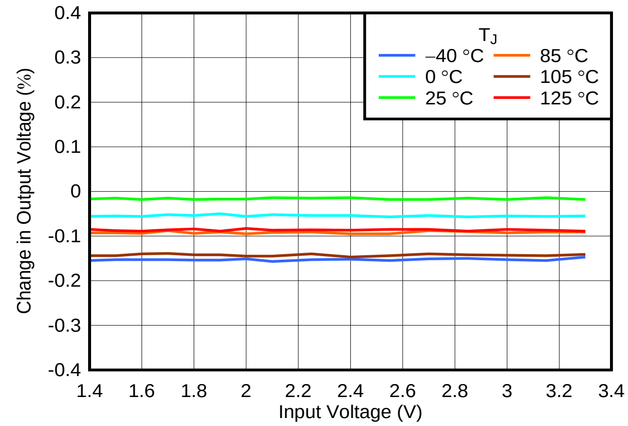
6.6 Typical Characteristics

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V, V_{BIAS} = $V_{OUT(NOM)}$ + 1.4 V, I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{IN} = C_{OUT} = 2.2 µF, and C_{BIAS} = 0.1 µF (unless otherwise noted)



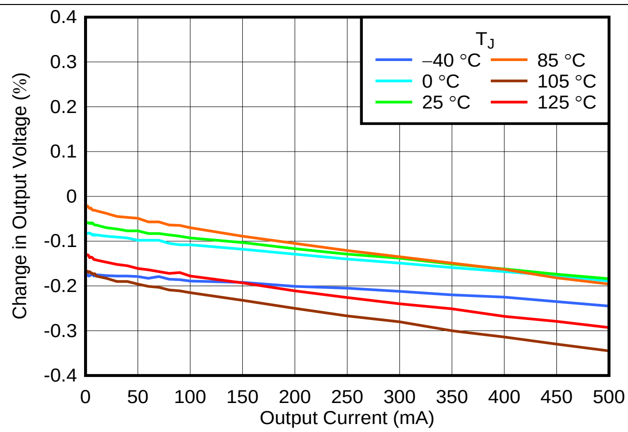
DRV package

Figure 1. Output Accuracy vs I_{OUT} and Temperature



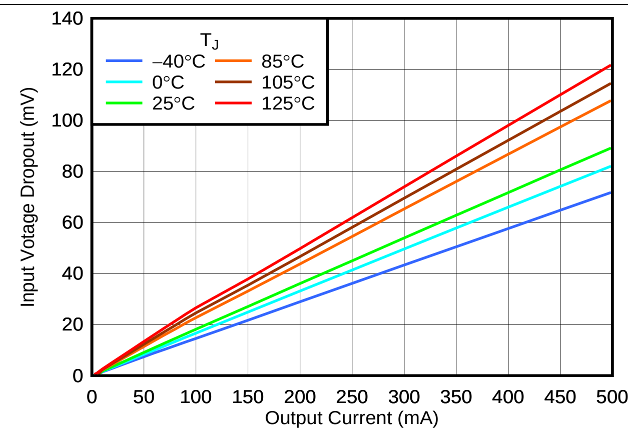
YKA package

Figure 2. Output Accuracy vs V_{IN} and Temperature



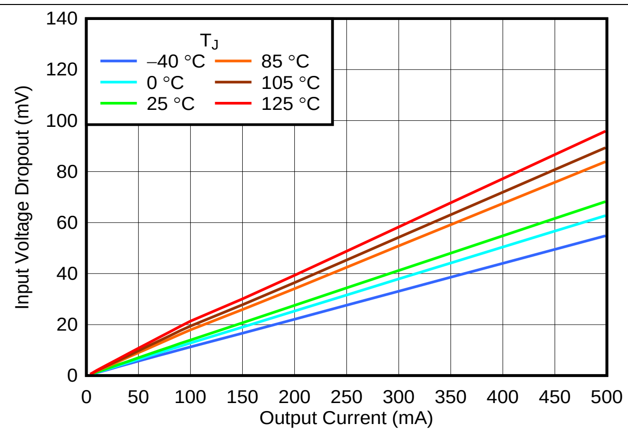
YKA package

Figure 3. Output Accuracy vs I_{OUT} and Temperature



DRV package

Figure 4. V_{IN} Dropout vs I_{OUT} and Temperature



YKA package

Figure 5. V_{IN} Dropout vs I_{OUT} and Temperature

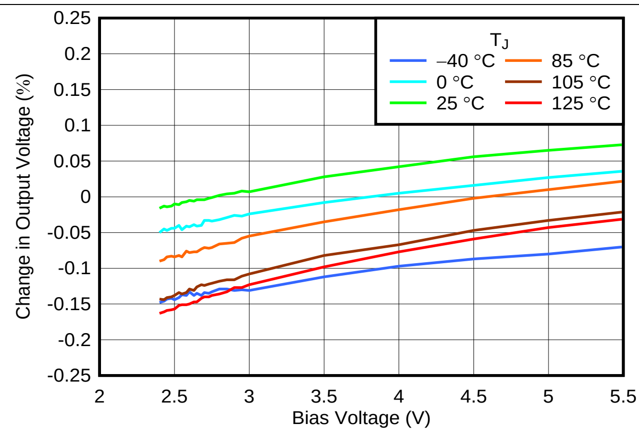


Figure 6. Output Accuracy vs V_{BIAS} and Temperature

Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V, V_{BIAS} = $V_{OUT(NOM)}$ + 1.4 V, I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{IN} = C_{OUT} = 2.2 µF, and C_{BIAS} = 0.1 µF (unless otherwise noted)

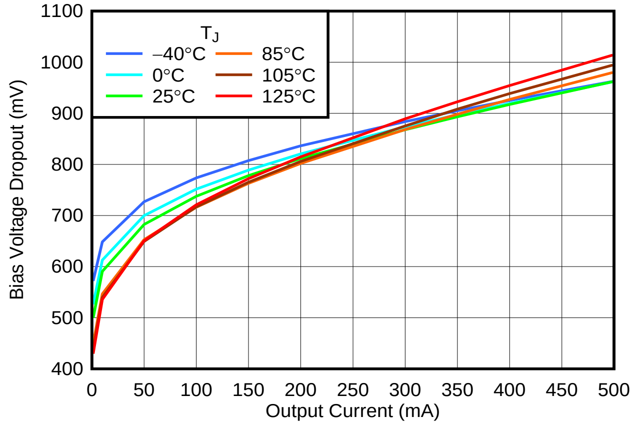


Figure 7. V_{BIAS} Dropout vs I_{OUT} and Temperature

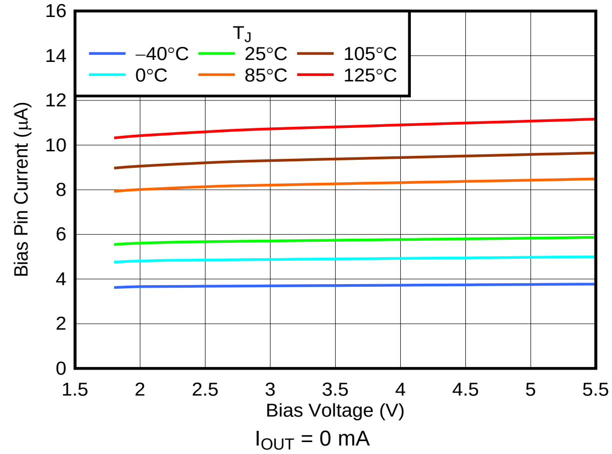


Figure 8. $I_{Q(BIAS)}$ vs V_{BIAS} and Temperature

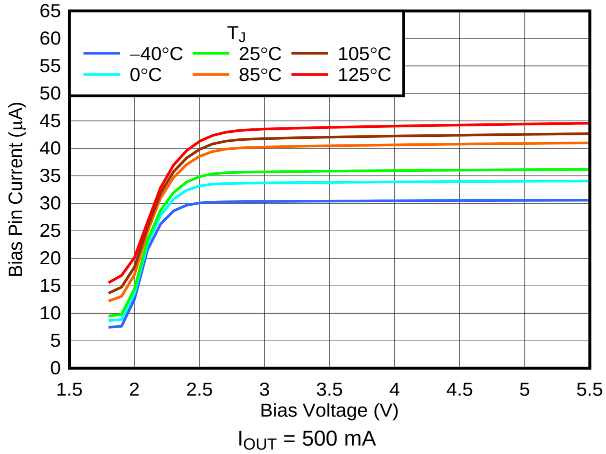


Figure 9. $I_{Q(BIAS)}$ vs V_{BIAS} and Temperature

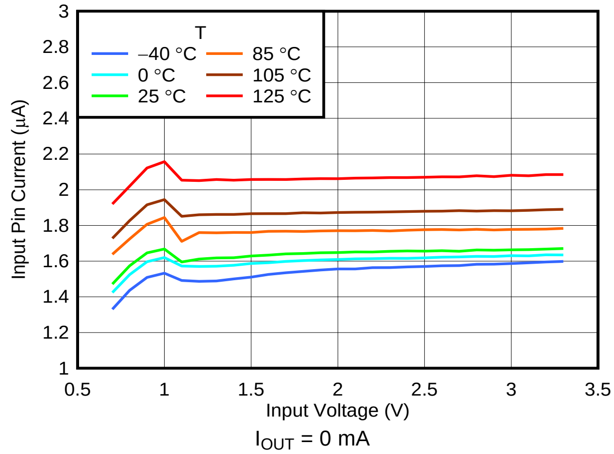


Figure 10. $I_{Q(IN)}$ vs V_{IN} and Temperature

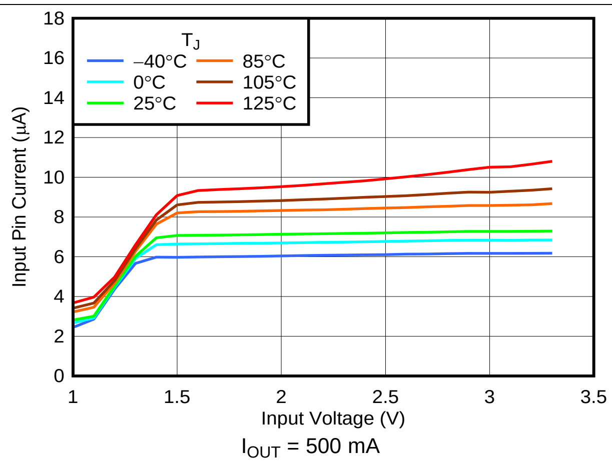


Figure 11. $I_{Q(IN)}$ vs V_{IN} and Temperature

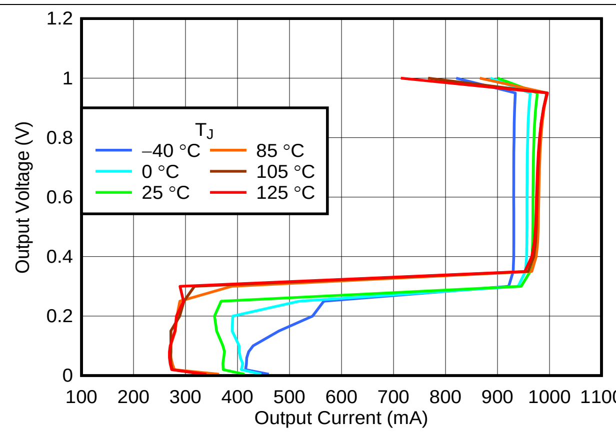
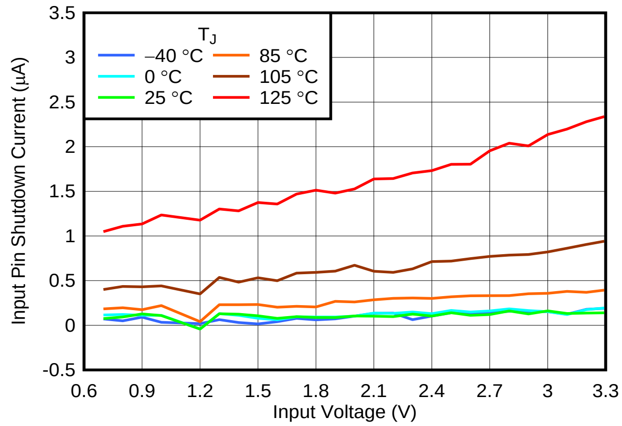


Figure 12. Foldback Output Current Limit vs I_{OUT} and Temperature

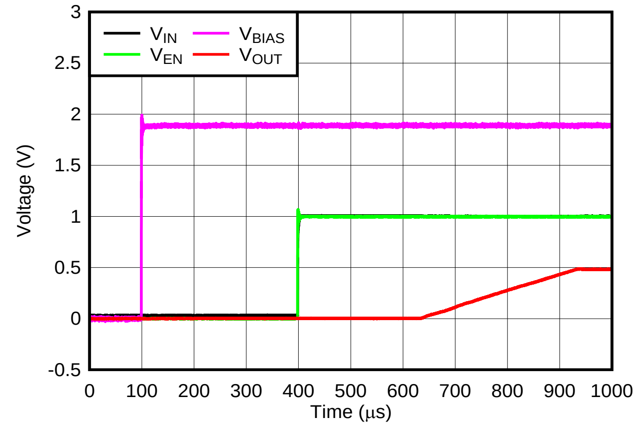
Typical Characteristics (continued)

at operating temperature T_J = 25°C, $V_{IN} = V_{OUT(NOM)}$ + 0.5 V, $V_{BIAS} = V_{OUT(NOM)}$ + 1.4 V, I_{OUT} = 1 mA, $V_{EN} = V_{IN}$, $C_{IN} = C_{OUT}$ = 2.2 µF, and C_{BIAS} = 0.1 µF (unless otherwise noted)



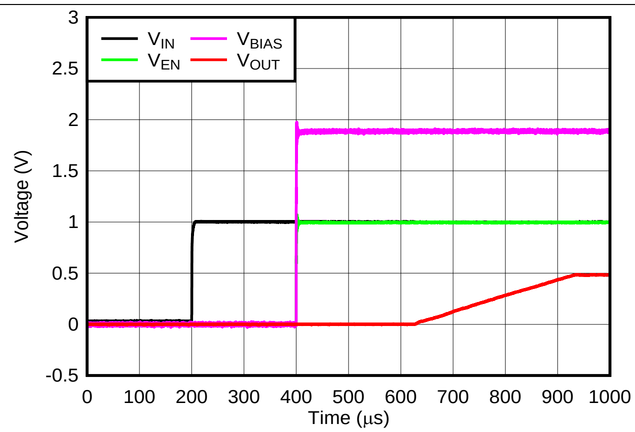
V_{OUT} = 1.0 V, V_{EN} < 0.4 V

Figure 13. I_{SHDN} vs V_{IN} and Temperature



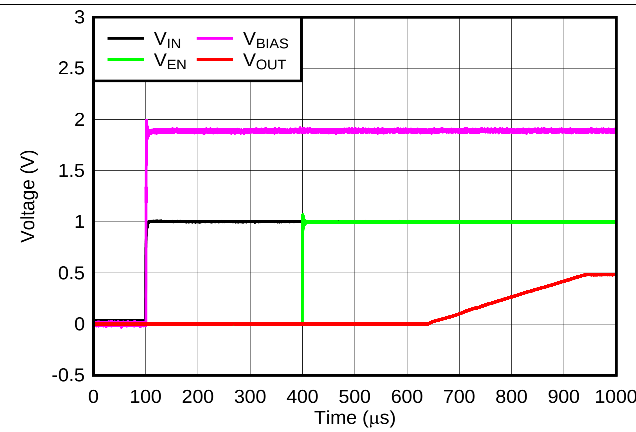
V_{OUT} = 0.5 V

Figure 14. Startup With $V_{EN} = V_{IN}$



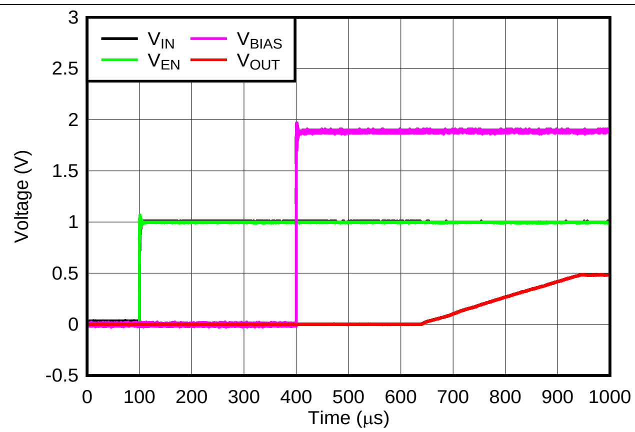
V_{OUT} = 0.5 V

Figure 15. Startup With V_{EN} and V_{BIAS} Powering Up Simultaneously



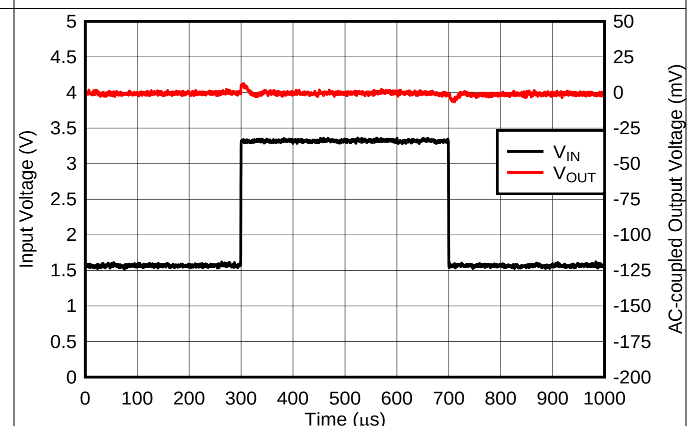
V_{OUT} = 0.5 V

Figure 16. Startup With Separated V_{EN}



V_{OUT} = 0.5 V

Figure 17. Startup With V_{BIAS} Powering Up After V_{IN} and V_{EN}

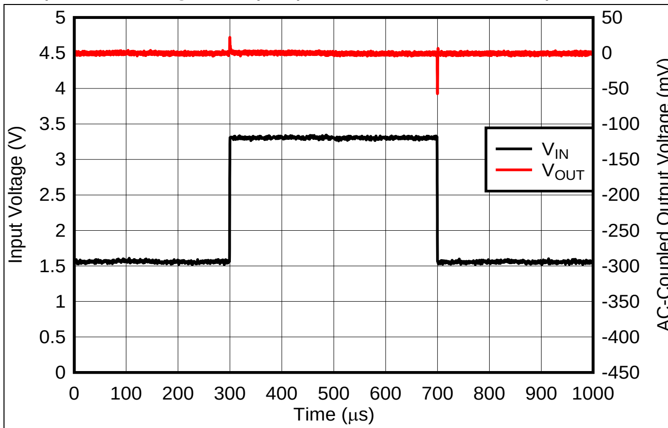


V_{OUT} = 1.0 V, I_{OUT} = 1 mA

Figure 18. V_{IN} Transient

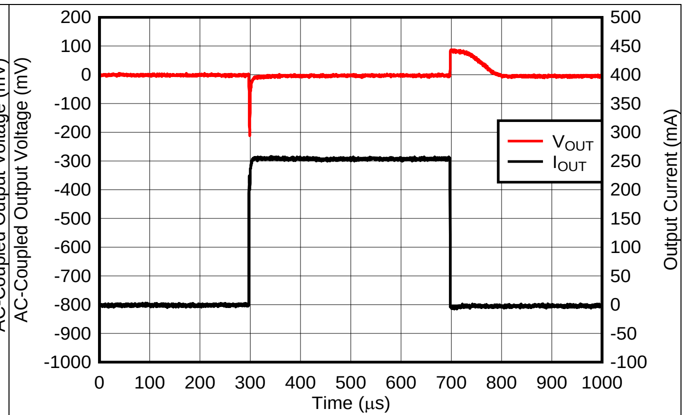
Typical Characteristics (continued)

at operating temperature T_J = 25°C, $V_{IN} = V_{OUT(NOM)}$ + 0.5 V, $V_{BIAS} = V_{OUT(NOM)}$ + 1.4 V, I_{OUT} = 1 mA, $V_{EN} = V_{IN}$, $C_{IN} = C_{OUT}$ = 2.2 µF, and C_{BIAS} = 0.1 µF (unless otherwise noted)



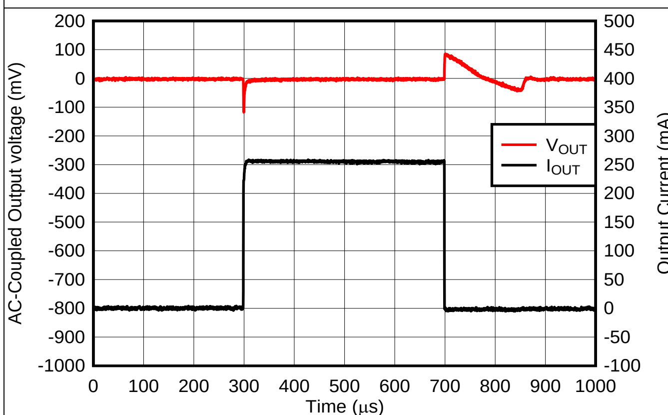
V_{OUT} = 1.0 V, I_{OUT} = 500 mA

Figure 19. V_{IN} Transient



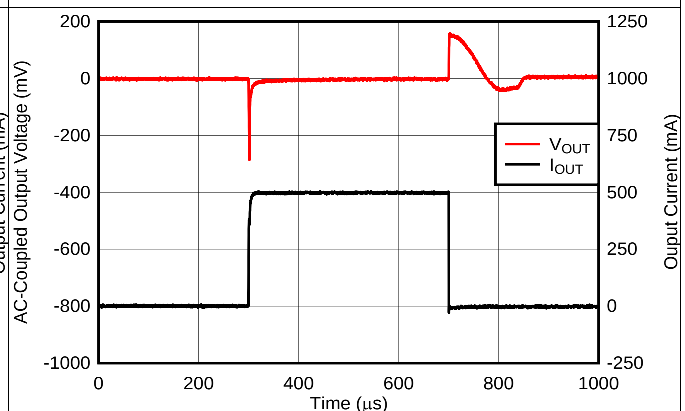
V_{OUT} = 1.0 V, I_{OUT} = 0 mA to 250 mA

Figure 20. I_{OUT} Transient



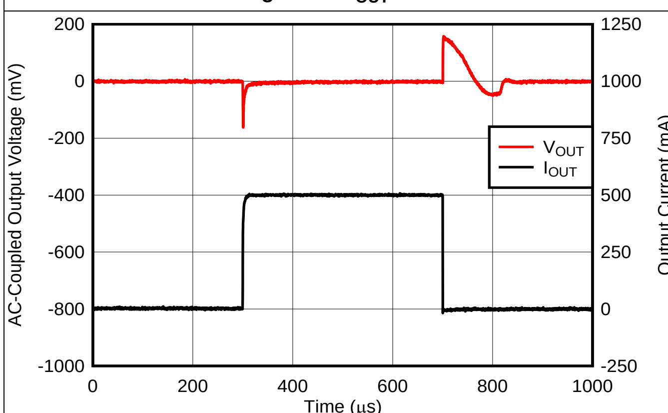
V_{OUT} = 1.0 V, I_{OUT} = 1 mA to 250 mA

Figure 21. I_{OUT} Transient



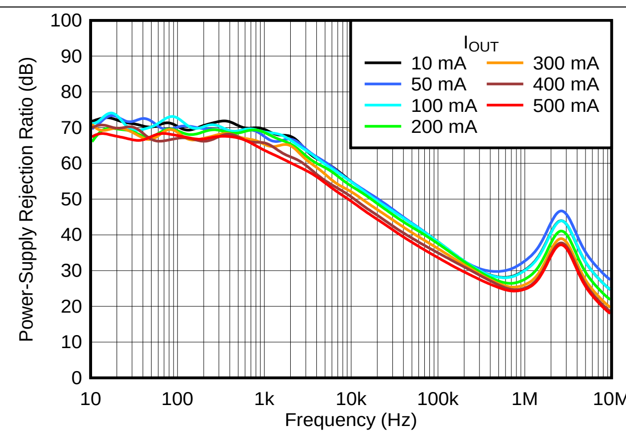
V_{OUT} = 1.0 V, I_{OUT} = 0 mA to 500 mA

Figure 22. I_{OUT} Transient



V_{OUT} = 1.0 V, I_{OUT} = 1 mA to 500 mA

Figure 23. I_{OUT} Transient

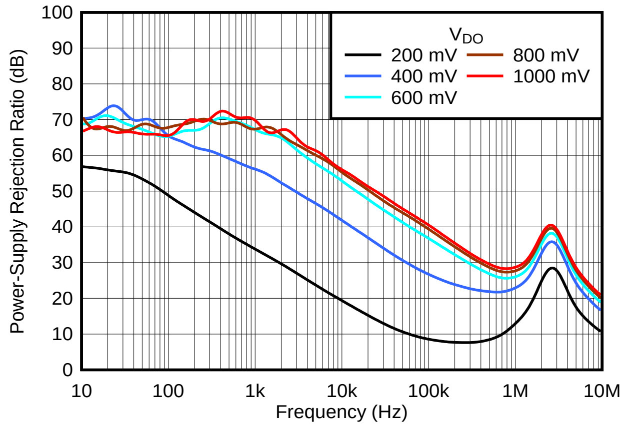


C_{IN} = 0 µF, V_{OUT} = 1.0 V

Figure 24. V_{IN} PSRR vs Frequency and I_{OUT}

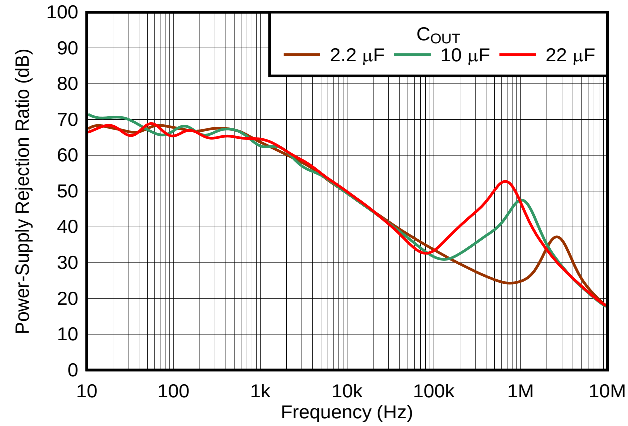
Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V, V_{BIAS} = $V_{OUT(NOM)}$ + 1.4 V, I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{IN} = C_{OUT} = 2.2 µF, and C_{BIAS} = 0.1 µF (unless otherwise noted)



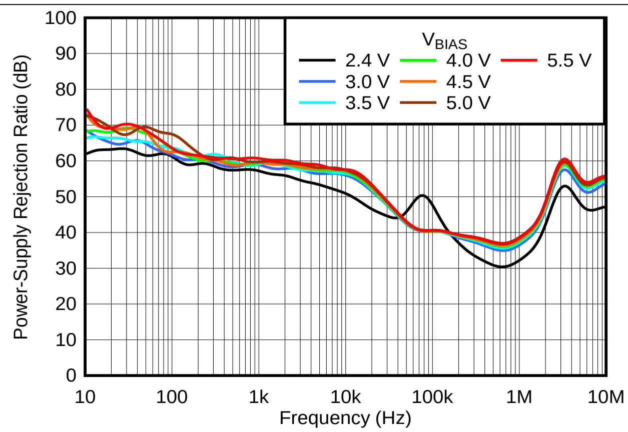
C_{IN} = 0 µF, V_{OUT} = 1.0 V, I_{OUT} = 500 mA, V_{DO} = V_{IN} – V_{OUT}

Figure 25. V_{IN} PSRR vs Frequency and Dropout



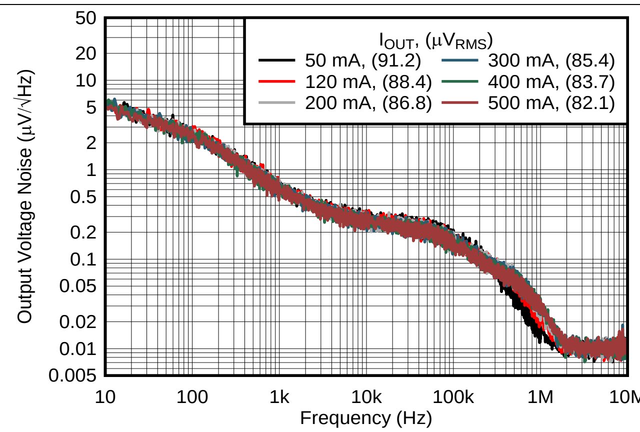
C_{IN} = 0 µF, V_{OUT} = 1.0 V, I_{OUT} = 500 mA

Figure 26. V_{IN} PSRR vs Frequency and C_{OUT}



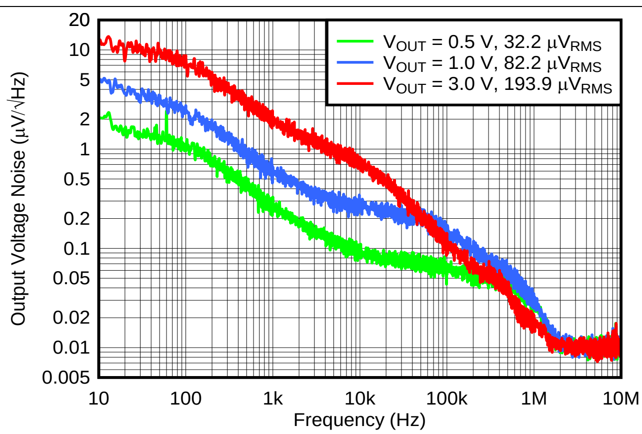
C_{IN} = 2.2 µF, V_{OUT} = 1.0 V, I_{OUT} = 500 mA, C_{BIAS} = 0 µF

Figure 27. V_{BIAS} PSRR vs Frequency and V_{BIAS}



V_{OUT} = 1.0 V

Figure 28. Output Noise vs Frequency and I_{OUT}



I_{OUT} = 500 mA

Figure 29. Output Noise vs Frequency and V_{OUT}

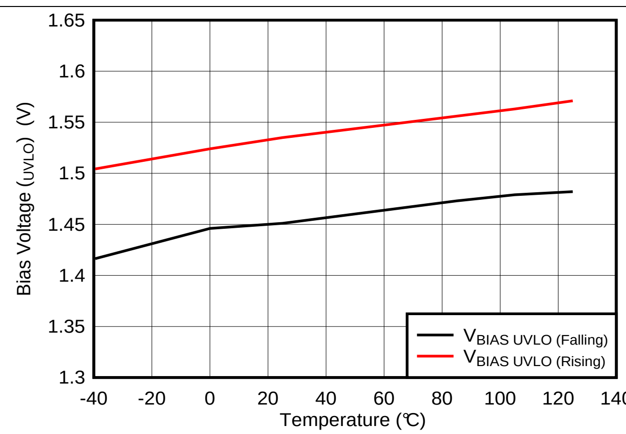


Figure 30. $V_{UVLO(BIAS)}$ Rising and Falling Threshold vs Temperature

Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V, V_{BIAS} = $V_{OUT(NOM)}$ + 1.4 V, I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{IN} = C_{OUT} = 2.2 µF, and C_{BIAS} = 0.1 µF (unless otherwise noted)

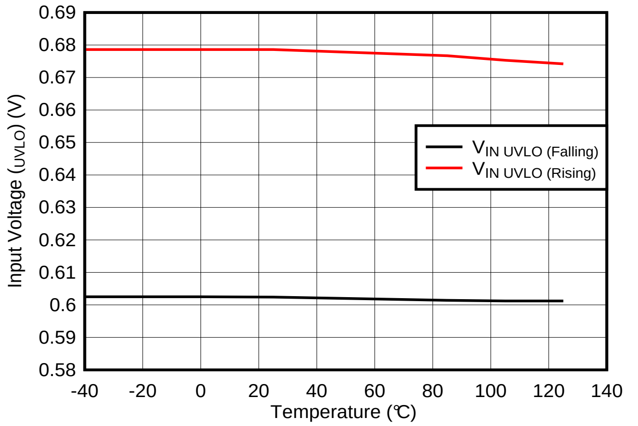


Figure 31. $V_{UVLO(IN)}$ Rising and Falling Threshold vs Temperature

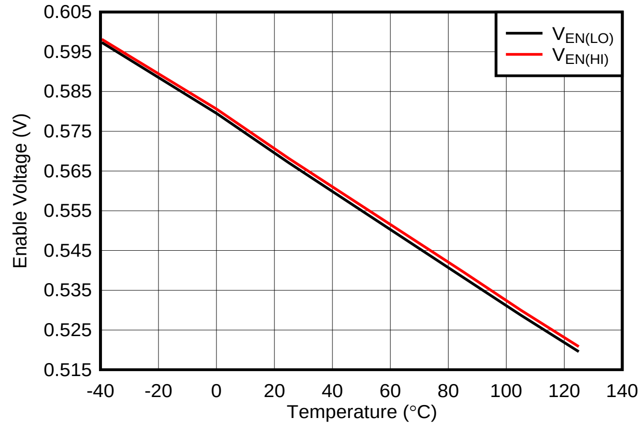


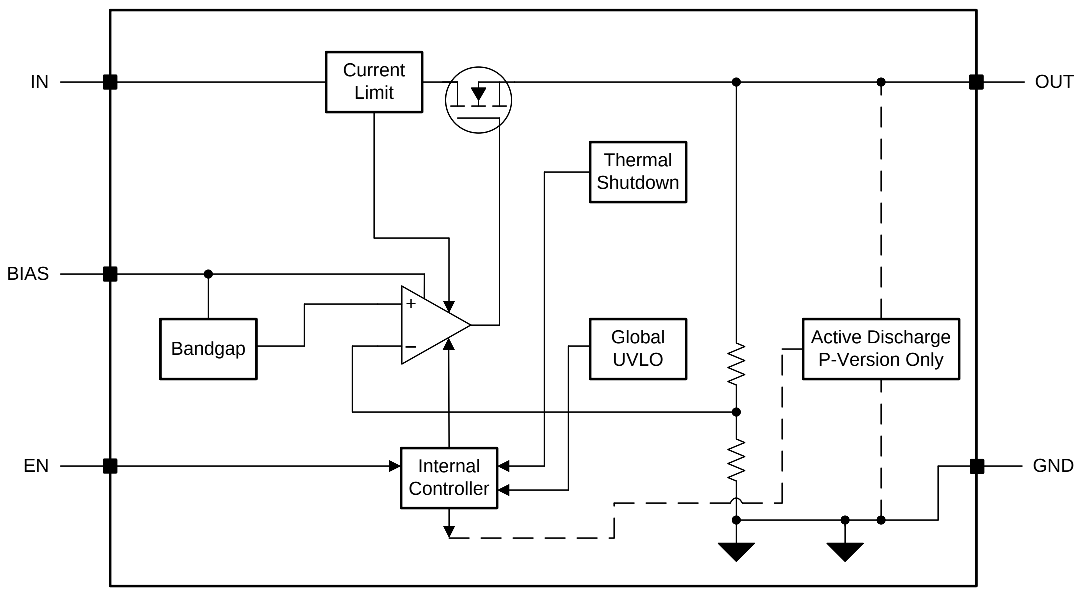
Figure 32. Enable High and Low Threshold vs Temperature

7 Detailed Description

7.1 Overview

The TPS7A11 is a low-input, ultra-low dropout, and low quiescent current linear regulator that is optimized for excellent transient performance. These characteristics make the device ideal for most battery-powered applications. The implementation of the BIAS pin on the TPS7A11 vastly improves efficiency of low-voltage output applications by allowing the use of a pre-regulated, low-voltage input supply that offers sub-band-gap output voltages. This low-dropout regulator (LDO) offers foldback current limit, shutdown, thermal protection, high output voltage accuracy of 1.5% over the recommended junction temperature range, and optional active discharge.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Excellent Transient Response

The TPS7A11 responds quickly to a transient on the input supply (line transient) or the output current (load transient) resulting from the device high input impedance and low output impedance across frequency. This same capability also means that the device has a high power-supply rejection ratio (PSRR) and low internal noise floor (e_n). The LDO approximates an ideal power supply with outstanding line and load transient performance.

The choice of external component values optimizes the small- and large-signal response; see the *Input and Output Capacitor Requirements* section for proper capacitor selection.

Feature Description (continued)

7.3.1.1 Global Undervoltage Lockout (UVLO)

The TPS7A11 uses two undervoltage lockout circuits: one on the BIAS pin and one on the IN pin to prevent the device from turning on before either V_{BIAS} and V_{IN} rise above their lockout voltages. The two UVLO signals are connected internally through an AND gate, as shown in Figure 33, that allows the device to be turned off when either of these rails are below the lockout voltage.

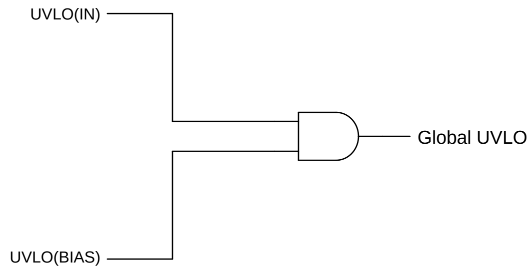


Figure 33. Global UVLO circuit

7.3.2 Active Discharge

The active discharge option has an internal pulldown MOSFET that connects a 120-Ω resistor to ground when the device is disabled in order to actively discharge the output voltage. The active discharge circuit is activated by driving the enable pin to logic low to disable the device, or when the device is in thermal shutdown.

The discharge time after disabling the device depends on the output capacitance (C_{OUT}) and the load resistance (R_L) in parallel with the 120-Ω pulldown resistor. Equation 1 calculates this time:

$$\tau = \frac{120 \cdot R_L}{120 + R_L} \cdot C_{OUT} \quad (1)$$

Do not rely on the active discharge circuit for discharging a large amount of output capacitance after the input supply has collapsed because reverse current can flow from the output to the input. This reverse current flow can cause damage to the device. Limit reverse current to no more than 5% of the device-rated current.

7.3.3 Enable Pin

The enable pin for the device is active high. The output of the device is turned on when the enable pin voltage is greater than the EN pin logic high voltage, and the output of the device is turned off when the enable pin voltage is less than the EN pin logic low voltage. A voltage less than the EN pin logic low voltage on the enable pin disables all internal circuits.

7.3.4 Sequencing Requirement

The IN, BIAS, and EN pin voltages can be sequenced in any order without causing damage to the device. The start up is always monotonic regardless of the sequencing order or the ramp rates of the IN, BIAS, and EN pins. For optimum device performance, V_{BIAS} should be present before enabling the device because the device internal circuitry is powered by V_{BIAS}; see the *Recommeded Operating Conditions* table for proper voltage ranges of the IN, BIAS, and EN pins.

7.3.5 Internal Foldback Current Limit

The internal foldback current limit circuit is used to protect the LDO against high-load current faults or shorting events. The foldback mechanism lowers the current limit as the output voltage decreases and limits power dissipation during short-circuit events, while still allowing for the device to operate at the rated output current; see Figure 12.

Feature Description (continued)

For example, when V_{OUT} is 90% of $V_{OUT(nom)}$, the current limit is I_{CL} (typical); however, if V_{OUT} is forced to 0 V, the current limit is I_{SC} (typical). In many LDOs, the foldback current limit can prevent start up into a constant-current load or a negatively-biased output. A brick-wall current limit is when there is an abrupt current stop after the current limit is reached. The foldback mechanism for this device goes into a brick-wall current limit when V_{OUT} is 90% of $V_{OUT(nom)}$, thus limiting current to I_{CL} (typical). When V_{OUT} is approximately 0 V, current is limited to I_{SC} (typical) in order to provide normal start up into a variety of loads. Thermal shutdown can be activated during a current-limit event because of the high power dissipation typically found in these conditions. To provide proper operation of the current limit, minimize the inductances to the input and load. Continuous operation in current limit is not recommended.

7.3.6 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the thermal junction temperature (T_J) of the main pass-FET rises to the thermal shutdown temperature (T_{SD}) for shutdown listed in the *Electrical Characteristics* table. Thermal shutdown hysteresis ensures that the LDO resets again (turns on) when the temperature falls to T_{SD} for reset.

The thermal time constant of the semiconductor die is fairly short, and thus the device may cycle on and off when thermal shutdown is reached until the power dissipation is reduced.

For reliable operation, limit the junction temperature to a maximum of 125°C. Operation above 125°C causes the device to exceed the operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overload conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above a junction temperature of 125°C reduces long-term reliability.

A fast start up when $T_J > T_{SD}$ for reset (typical, outside of the specified operation range) causes the device thermal shutdown to assert at T_{SD} for reset, and prevents the device from turning on until the junction temperature is reduced below T_{SD} for reset.

7.4 Device Functional Modes

The device has the following modes of operation:

- Normal operation: The device regulates to the nominal output voltage
- Dropout operation: The pass element operates as a resistor and the output voltage is set as $V_{IN} – V_{DO}$
- Disabled: The output of the device is disabled and the discharge circuit is activated

Table 1 shows the conditions that lead to the different modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER				
	V_{IN}	V_{BIAS}	V_{EN}	I_{OUT}	T_J
Normal mode	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{BIAS} > V_{OUT} + V_{DO(BIAS)}$	$V_{EN} > V_{HI(EN)}$	$I_{OUT} < I_{CL}$	$T_J < T_{SD}$ for shutdown
Dropout mode	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO(IN)}$	$V_{BIAS} < V_{OUT} + V_{DO(BIAS)}$	$V_{EN} > V_{HI(EN)}$	$I_{OUT} < I_{CL}$	$T_J < T_{SD}$ for shutdown
Disabled mode (any true condition disables the device)	$V_{IN} < V_{UVLO(IN)}$	$V_{BIAS} < V_{BIAS(UVLO)}$	$V_{EN} < V_{LO(EN)}$	—	$T_J > T_{SD}$ for shutdown

7.4.1 Normal Mode

The device regulates the output to the nominal output voltage when all normal mode conditions in Table 1 are met.

7.4.2 Dropout Mode

The device is not in regulation, and the output voltage tracks the input voltage minus the voltage drop across the pass element of the device. In this mode, the PSRR, noise, and transient performance of the device are significantly degraded.

7.4.3 Disable Mode

In this mode the pass element is turned off, the internal circuits are shut down, and the output voltage is actively discharged to ground by an internal resistor.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

Successfully implementing an LDO in an application depends on the application requirements. This section discusses key device features and how to best implement them to achieve a reliable design.

8.1.1 Recommended Capacitor Types

The device is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input, output, and bias pins. Multilayer ceramic capacitors are the industry standard for these types of applications, but must be used with good judgment. Ceramic capacitors that use X7R-, X5R-, and COG-rated dielectric materials provide relatively good capacitive stability across temperature. Avoid Y5V-rated capacitors because of large variations in capacitance. Regardless of the ceramic capacitor type selected, ceramic capacitance varies with operating voltage and temperature. As a rule of thumb, assume that effective capacitance decreases by as much as 50%. The input, output, and bias capacitors recommended in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.

8.1.2 Input and Output Capacitor Requirements

A minimum input ceramic capacitor is required for stability. A minimum output ceramic capacitor is also required for stability, refer to the *Recommended Operating Conditions* table for the minimum capacitors values.

The input capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. A higher-value input capacitor may be necessary if large, fast rise-time load or line transients are anticipated, or if the device is located several inches from the input power source. Dynamic performance of the device is improved with the use of an output capacitor larger than the minimum value specified in the *Recommended Operating Conditions* table.

Although a bias capacitor is not required, connect a 0.1-µF ceramic capacitor from BIAS to GND for best analog design practice. This capacitor counteracts reactive bias sources if the source impedance is not sufficiently low. Place the input, output, and bias capacitors as close as possible to the device to minimize trace parasitics.

8.1.3 Load Transient Response

The load-step transient response is the output voltage response by the LDO to a step in load current while output voltage regulation is maintained. See Figure 20 to Figure 23 for typical load transient response. There are two key transitions during a load transient response: the transition from a light to a heavy load, and the transition from a heavy to a light load. The regions in Figure 34 are broken down as described in this section. Regions A, E, and H are where the output voltage is in steady-state operation.

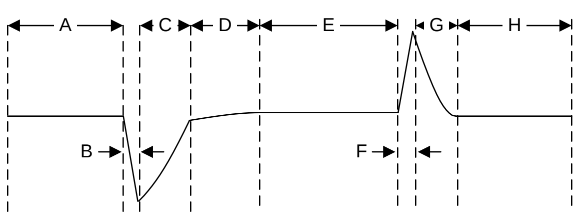


Figure 34. Load Transient Waveform

Application Information (continued)

During transitions from a light load to a heavy load, the:

- Initial voltage dip is a result of the depletion of the output capacitor charge and parasitic impedance to the output capacitor (region B)
- Recovery from the dip results from the LDO increasing the sourcing current, and leads to output voltage regulation (region C)

During transitions from a heavy load to a light load, the:

- Initial voltage rise results from the LDO sourcing a large current, and leads to an increase in the output capacitor charge (region F)
- Recovery from the rise results from the LDO decreasing its sourcing current in combination with the load discharging the output capacitor (region G)

A larger output capacitance reduces the peaks during a load transient but slows down the response time of the device. A larger dc load also reduces the peaks because the amplitude of the transition is lowered and a higher current discharge path is provided for the output capacitor.

8.1.4 Dropout Voltage

Generally, the dropout voltage often refers to the minimum voltage difference between the input and output voltage ($V_{DO} = V_{IN} – V_{OUT}$) that is required for regulation. When $V_{IN} – V_{OUT}$ drops below the required V_{DO} for the given load current, the device functions as a resistive switch and does not regulate output voltage. Dropout voltage is linearly proportional to the output current because the device is operating as a resistive switch, see Figure 4 and Figure 5.

Dropout voltage is also affected by the drive strength for the gate of the pass element, which is nonlinear with respect to V_{BIAS} on this device because of the inherited nonlinearity of the pass element gate capacitance, see Figure 7.

8.1.5 Behavior During Transition From Dropout Into Regulation

Some applications may have transients that place this device into dropout, especially when this device can be powered from a battery with relatively high ESR. The load transient saturates the output stage of the error amplifier when the pass element is driven fully on, making the pass element function like a resistor from V_{IN} to V_{OUT}. The error amplifier response time to this load transient is limited because the error amplifier must first recover from saturation and then places the pass element back into active mode. During this time, V_{OUT} overshoots because the pass element is functioning as a resistor from V_{IN} to V_{OUT}.

When V_{IN} ramps up slowly for start-up, the slow ramp-up voltage may place the device in dropout. As with many other LDOs, the output can overshoot on recovery from this condition. However, this condition is easily avoided through the use of the enable signal.

If operating under these conditions, apply a higher dc load or increase the output capacitance to reduce the overshoot. These solutions provide a path to dissipate the excess charge.

8.1.6 Undervoltage Lockout Circuit Operation

The V_{IN} UVLO circuit makes sure that the device remains disabled before the input supply reaches the minimum operational voltage range. The V_{IN} UVLO circuit also makes sure that the device shuts down when the input supply collapses. Similarly, the V_{BIAS} UVLO circuit makes sure that the device stays disabled before the bias supply reaches the minimum operational voltage range. The V_{BIAS} UVLO circuit also makes sure that the device shuts down when the bias supply collapses.

Figure 35 depicts the UVLO circuit response to various input or bias voltage events. The diagram can be separated into the following parts:

- Region A: The device does not start until the input or bias voltage reaches the UVLO rising threshold
- Region B: Normal operation, regulating device
- Region C: Brownout event above the UVLO falling threshold (UVLO rising threshold – UVLO hystersis). The output may fall out of regulation but the device is still enabled.
- Region D: Normal operation, regulating device
- Region E: Brownout event below the UVLO falling threshold. The device is disabled in most cases and the

Application Information (continued)

output falls as a result of the load and active discharge circuit. The device is re-enabled when the UVLO rising threshold is reached and a normal start-up follows.

- Region F: Normal operation followed by the input or bias falling to the UVLO falling threshold
- Region G: The device is disabled when the input or bias voltages fall below the UVLO falling threshold to 0 V. The output falls as a result of the load and active discharge circuit.

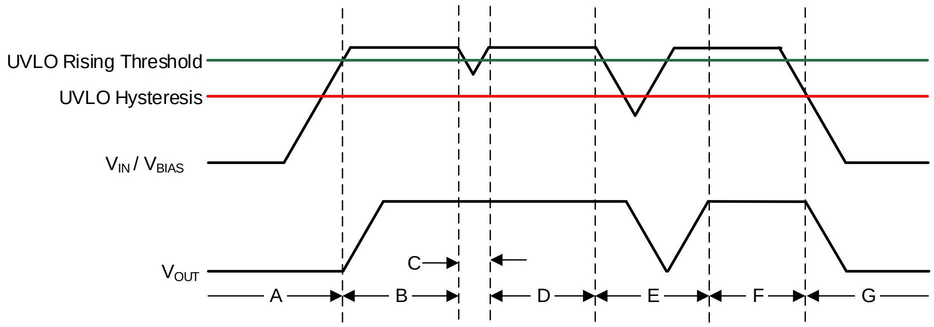


Figure 35. Typical V_{IN} or V_{BIAS} UVLO Circuit Operation

8.1.7 Power Dissipation (P_D)

Circuit reliability demands that proper consideration be given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must be as free as possible of other heat-generating devices that cause added thermal stresses.

Equation 2 calculates the maximum allowable power dissipation for the device in a given package:

$$P_{D\text{-}MAX} = [(T_J – T_A) / R_{\theta JA}] \quad (2)$$

Equation 3 represents the actual power being dissipated in the device:

$$P_D = (I_{GND} + I_{OUT}) \times (V_{IN} – V_{OUT}) \quad (3)$$

Power dissipation can be minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input-to-output voltage differential to be obtained. The low dropout of the TPS7A11 allows for maximum efficiency across a wide range of output voltages.

The main heat conduction path for the device depends on the ambient temperature and the thermal resistance across the various interfaces between the die junction and ambient air.

The maximum power dissipation determines the maximum allowable junction temperature (T_J) for the device. According to Equation 4, maximum power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A). The equation is rearranged in Equation 5 for output current.

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (4)$$

$$I_{OUT} = (T_J – T_A) / [R_{\theta JA} \times (V_{IN} – V_{OUT})] \quad (5)$$

Unfortunately, this thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in the *Electrical Characteristics* table is determined by the JEDEC standard, PCB, and copper-spreading area, and is only used as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the DRV package junction-to-case (bottom) thermal resistance ($R_{\theta JC(bot)}$) plus the thermal resistance contribution by the PCB copper.

Application Information (continued)

8.1.8 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of the copper-spreading area. The key thermal metrics (Ψ_{JT} and Ψ_{JB}) are used in accordance with Equation 6 and are given in the *Electrical Characteristics* table.

$$\Psi_{JT} : T_J = T_T + \Psi_{JT} \times P_D \text{ and } \Psi_{JB} : T_J = T_B + \Psi_{JB} \times P_D \quad (6)$$

where:

- P_D is the power dissipated as explained in Equation 3
- T_T is the temperature at the center-top of the device package
- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

8.1.9 Recommended Area for Continuous Operation

The operational area of an LDO is limited by the dropout voltage, output current, junction temperature, and input voltage. The recommended area for continuous operation for a linear regulator is shown in Figure 36 and can be separated into the following regions:

- Dropout voltage limits the minimum differential voltage between the input and the output (V_{IN} – V_{OUT}) at a given output current level; see the *Dropout Voltage* section for more details.
- The rated output current limits the maximum recommended output current level. Exceeding this rating causes the device to fall out of specification.
- The rated junction temperature limits the maximum junction temperature of the device. Exceeding this rating causes the device to fall out of specification and reduces long-term reliability.
  - Equation 5 provides the shape of the slope. The slope is nonlinear because the maximum rated junction temperature of the LDO is controlled by the power dissipation across the LDO, thus when V_{IN} – V_{OUT} increases the output current must decrease.
- The rated input voltage range governs both the minimum and maximum of V_{IN} – V_{OUT}.

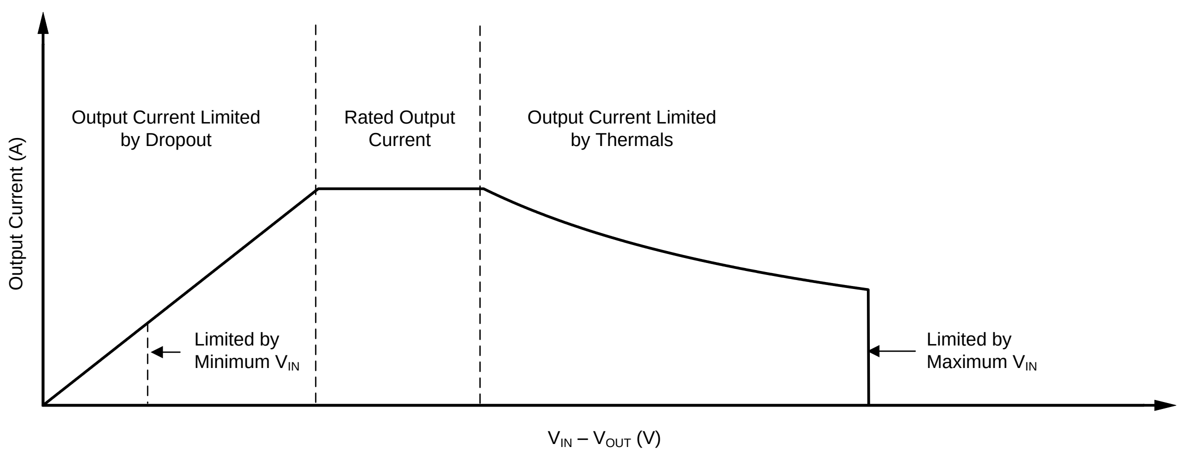


Figure 36. Continuous Operation Diagram With Description of Regions

8.2 Typical Application

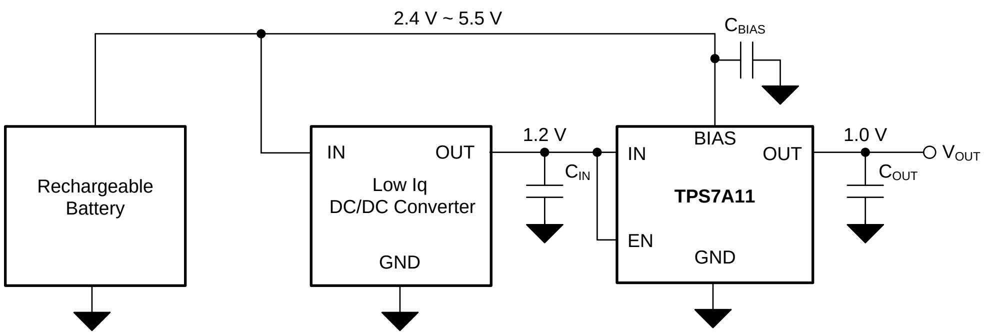


Figure 37. High Efficiency Supply From a Rechargeable Battery

8.2.1 Design Requirements

Table 2 lists the parameters for this design example.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	1.2 V
V_{BIAS}	2.4 V (min)
V_{OUT}	1.0 V
I_{OUT}	150 mA (typical), 500 mA (peak)

8.2.2 Detailed Design Procedures

This design example is powered by a rechargeable battery that can be a building block in many portable applications. Noise-sensitive portable electronics require an efficient small-size solution for their power supply. Traditional LDOs are known for their low efficiency in contrast to the low-input, low-output voltage (LILO) LDOs such as the TPS7A11. The use of a bias rail in the TPS7A11 allows the device to operate at a lower input voltage, thus reducing the power dissipation across the die and maximizing device efficiency. Equation 7 calculates the efficiency for this design.

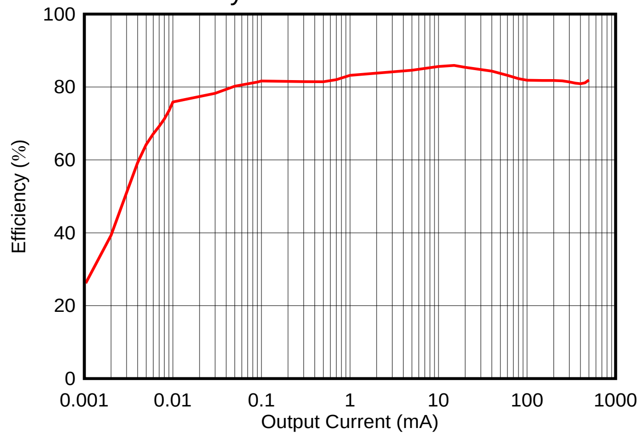
$$\text{Efficiency} = \eta = P_{OUT}/P_{IN} \times 100\ \% = (V_{OUT} \times I_{OUT}) / (V_{IN} \times I_{IN} + V_{BIAS} \times I_{BIAS}) \times 100\ \% \quad (7)$$

Equation 7 reduces to Equation 8 because the design example load current is much greater than the quiescent current of the bias rail.

$$\text{Efficiency} = \eta = (V_{OUT} \times I_{OUT}) / (V_{IN} \times I_{IN}) \times 100\% \quad (8)$$

8.2.3 Application Curve

Figure 38 shows a plot of the calculated efficiency.



$V_{IN} = V_{EN} = 1.2$ V, $C_{IN} = 2.2$ µF, $V_{OUT} = 1.0$ V, $C_{OUT} = 2.2$ µF, $V_{BIAS} = 2.4$ V, $C_{BIAS} = 0.1$ µF

Figure 38. TPS7A11 Output Efficiency at 1.2 V_{IN} and 1.0 V_{OUT}

9 Power Supply Recommendations

This device is designed to operate from an input supply voltage range of 0.75 V to 3.3 V and a bias supply voltage range of 1.7 V to 5.5 V. The input and bias supplies must be well regulated and free of spurious noise. To make sure that the output voltage is well regulated and dynamic performance is optimum, the input supply must be at least $V_{OUT(nom)}$ + 0.5 V and $V_{BIAS} = V_{OUT(nom)} + V_{DO(BIAS)}$.

10 Layout

10.1 Layout Guidelines

For correct printed circuit board (PCB) layout, follow these guidelines:

- Place input, output, and bias capacitors as close to the device as possible
- Use copper planes for device connections to optimize thermal performance
- Place thermal vias around the device to distribute heat

10.2 Layout Examples

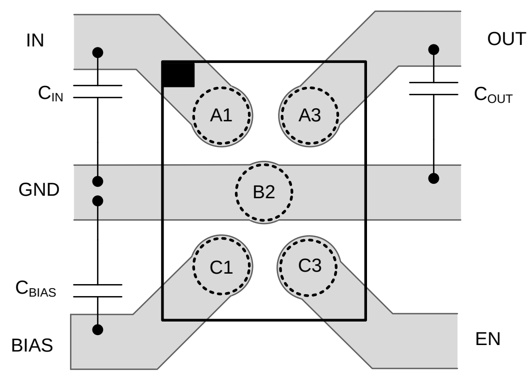


Figure 39. Recommended Layout for YKA Package

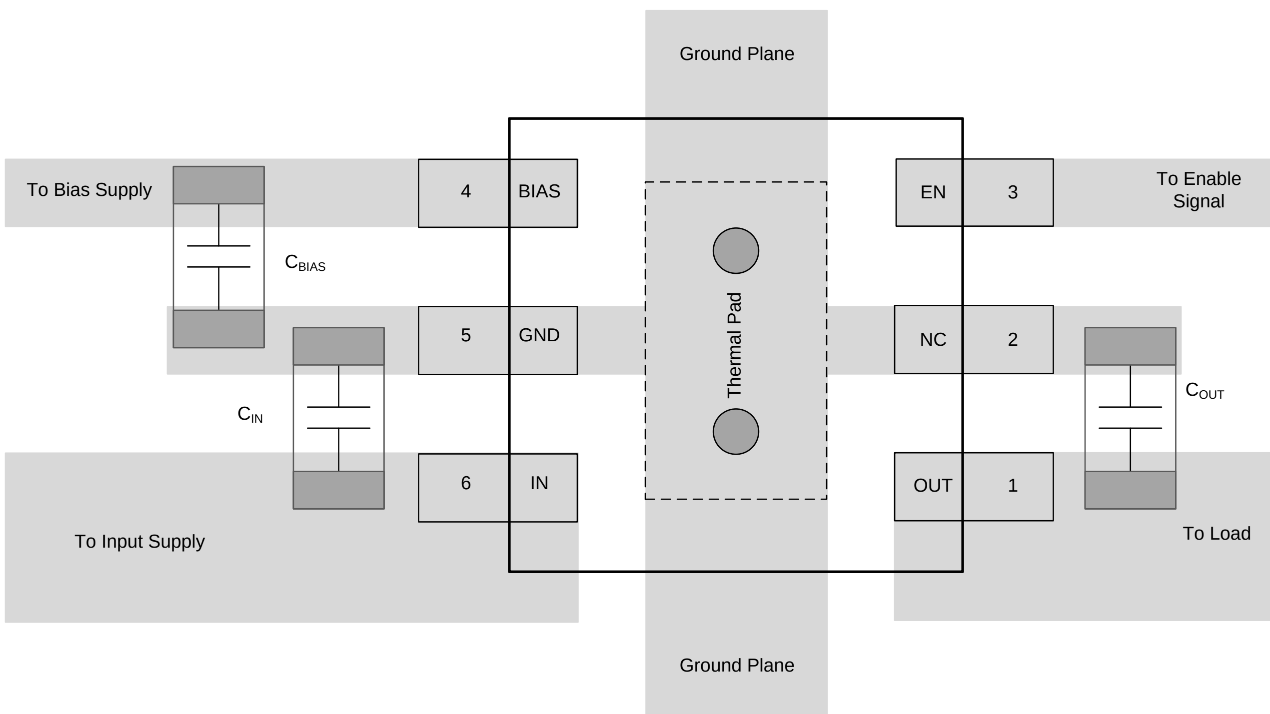


Figure 40. Recommended Layout for DRV Package

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Evaluation Module

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS7A11. The TPS720xxDRVEVM evaluation module (and related user guide) can be requested at the Texas Instruments website through the product folders or purchased directly from the TI eStore.

11.1.2 Spice Model

Spice models for this device are available through the for the TPS7A11 product folder under the *Tool and Software* tab.

11.1.3 Device Nomenclature

Table 3. Device Nomenclature(1)(2)

PRODUCT	V_{OUT}
TPS7A11**xx(x)**	**xx(x)** is the nominal output voltage. For output voltages with a resolution of 50 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 28 = 2.8 V; 125 = 1.25 V). **yyy** is the package designator. **z** is the package quantity. R is for reel (3000 pieces), T is for tape (250 pieces).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.
(2) Output voltages from 0.5 V to 3.0 V in 50-mV increments are available. Contact the factory for details and availability.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *TPS720xxDRVEVM Evaluation Module*
- *Using New Thermal Metrics Application Report*
- *AN-1112 DSBGA Wafer Level Chip Scale Package Application Report*
- *Light Load Efficient, Low Noise Power Supply Reference Design for Wearables and IoT*

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A1106PDRVR	PREVIEW	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1R6H	
TPS7A1106PDRVT	PREVIEW	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1R6H	
TPS7A1108PDRVR	PREVIEW	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1R7H	
TPS7A1108PDRVT	PREVIEW	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1R7H	
TPS7A11105PDRVR	PREVIEW	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1R9H	
TPS7A11105PDRVT	PREVIEW	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1R9H	
TPS7A1110PDRVR	PREVIEW	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1R8H	
TPS7A1110PDRVT	PREVIEW	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1R8H	
TPS7A1111PDRVR	PREVIEW	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1RAH	
TPS7A1111PDRVT	PREVIEW	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1RAH	
TPS7A1112PDRVR	PREVIEW	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1RBH	
TPS7A1112PDRVT	PREVIEW	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1RBH	
TPS7A1115PDRVR	PREVIEW	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1RCH	
TPS7A1115PDRVT	PREVIEW	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1RCH	
TPS7A1118PDRVR	PREVIEW	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1RDH	
TPS7A1118PDRVT	PREVIEW	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1RDH	
TPS7A1125PDRVR	PREVIEW	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125		

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A1125PDRVT	PREVIEW	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1REH	
TPS7A1128PDRVR	PREVIEW	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1RFH	
TPS7A1128PDRVT	PREVIEW	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1RFH	
TPS7A1130PDRVR	PREVIEW	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1RGH	
TPS7A1130PDRVT	PREVIEW	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1RGH	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

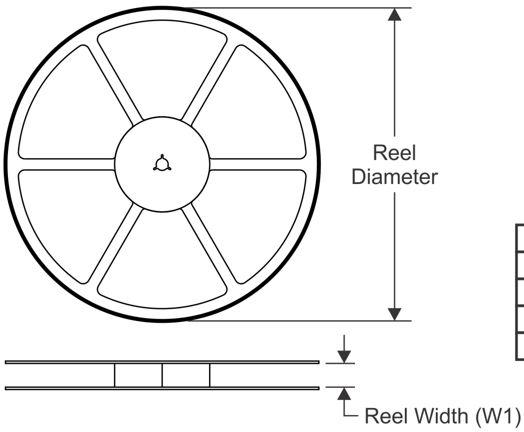
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

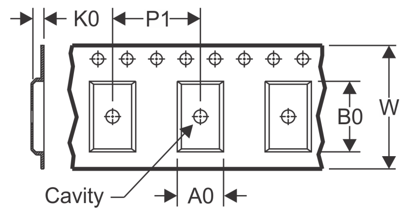
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

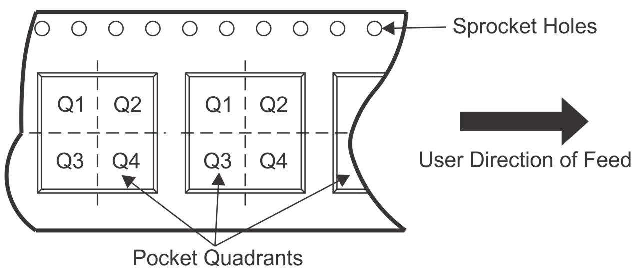


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

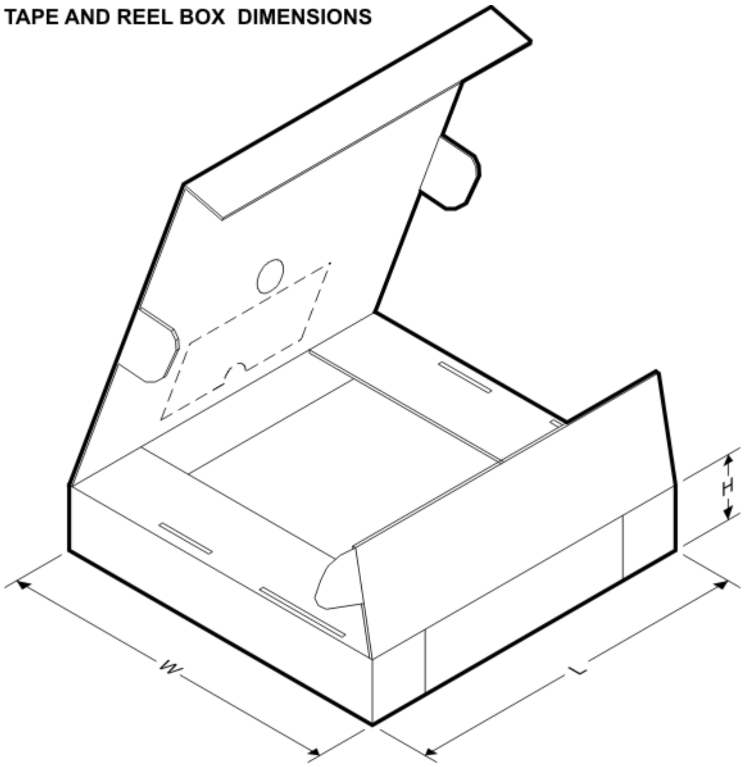


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A1106PDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS7A1106PDRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS7A1108PDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS7A1108PDRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS7A11105PDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS7A11105PDRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS7A1110PDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS7A1110PDRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS7A1111PDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS7A1111PDRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS7A1112PDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS7A1112PDRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS7A1115PDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS7A1115PDRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS7A1118PDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS7A1118PDRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS7A1125PDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS7A1125PDRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A1128PDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS7A1128PDRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS7A1130PDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS7A1130PDRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



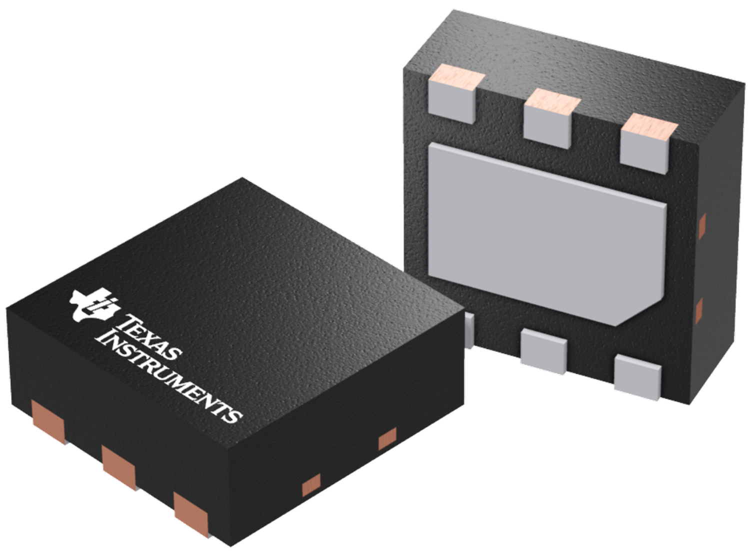
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A1106PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TPS7A1106PDRVT	WSON	DRV	6	250	210.0	185.0	35.0
TPS7A1108PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TPS7A1108PDRVT	WSON	DRV	6	250	210.0	185.0	35.0
TPS7A11105PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TPS7A11105PDRVT	WSON	DRV	6	250	210.0	185.0	35.0
TPS7A1110PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TPS7A1110PDRVT	WSON	DRV	6	250	210.0	185.0	35.0
TPS7A1111PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TPS7A1111PDRVT	WSON	DRV	6	250	210.0	185.0	35.0
TPS7A1112PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TPS7A1112PDRVT	WSON	DRV	6	250	210.0	185.0	35.0
TPS7A1115PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A1115PDRVT	WSON	DRV	6	250	210.0	185.0	35.0
TPS7A1118PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TPS7A1118PDRVT	WSON	DRV	6	250	210.0	185.0	35.0
TPS7A1125PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TPS7A1125PDRVT	WSON	DRV	6	250	210.0	185.0	35.0
TPS7A1128PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TPS7A1128PDRVT	WSON	DRV	6	250	210.0	185.0	35.0
TPS7A1130PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TPS7A1130PDRVT	WSON	DRV	6	250	210.0	185.0	35.0

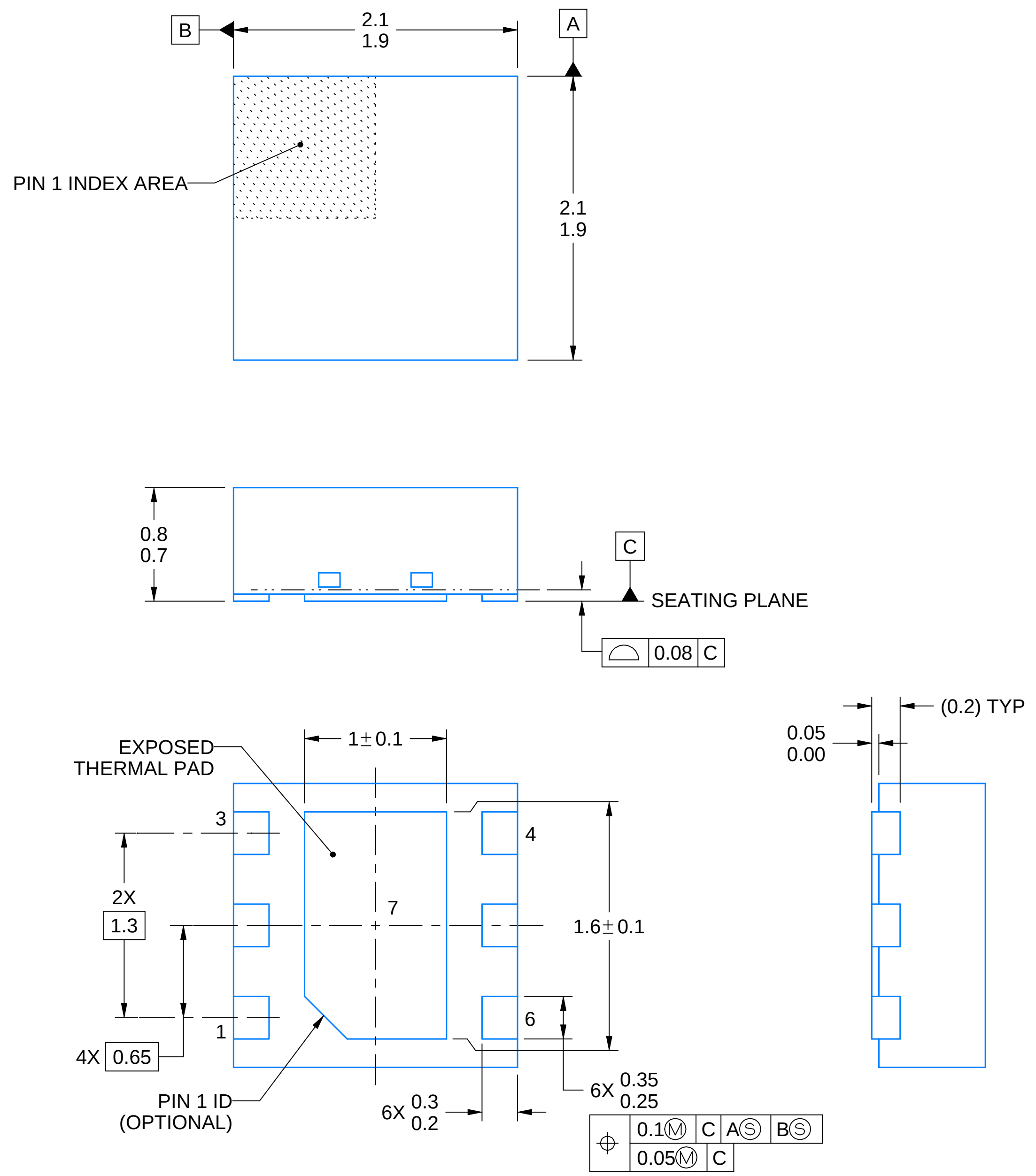
DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

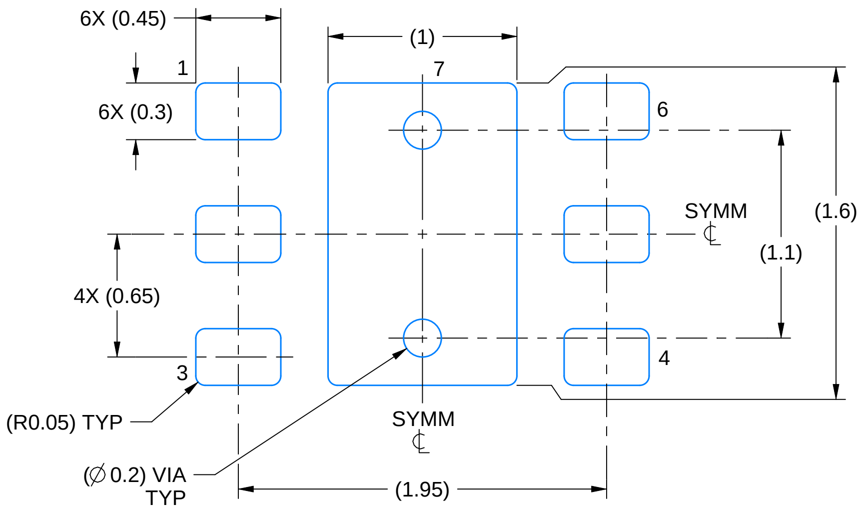
4206925/F



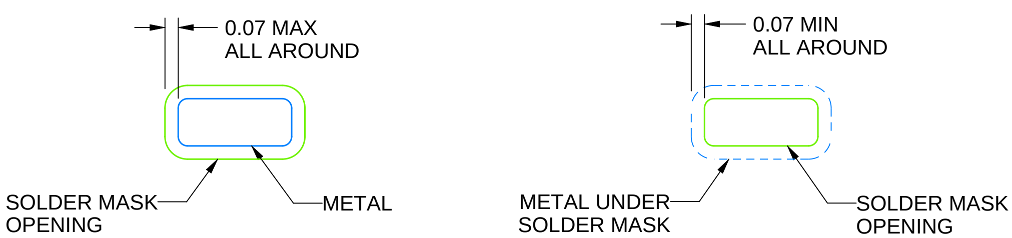
4222173/B 04/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:25X



NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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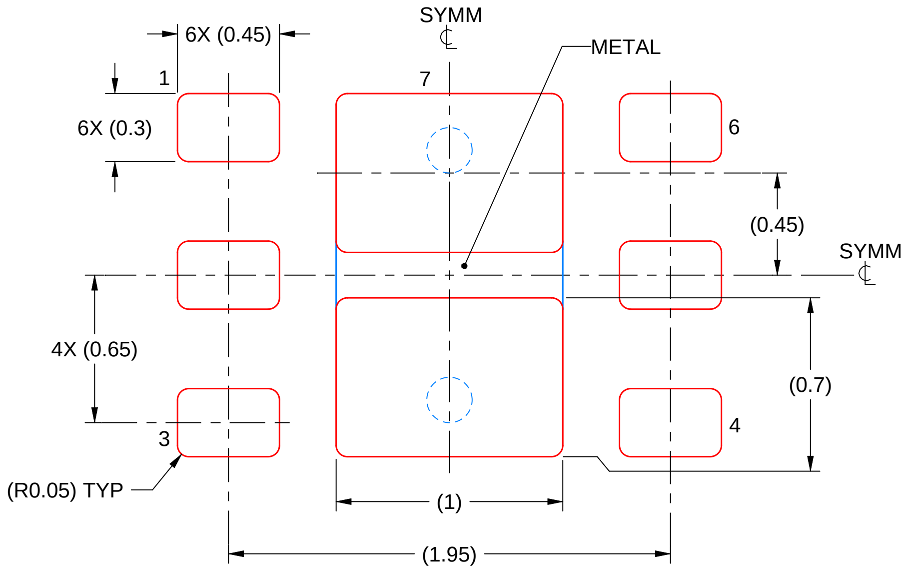
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/B 04/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.